What is claimed is:

1. An input and output circuit of a semiconductor device, comprising:

a control signal generating means for generating a first control signal of a power supply voltage, a second control signal of a ground voltage and a third control signal of a high voltage greater than the power supply voltage, respectively, when the high voltage is applied to a pad of the semiconductor device under a power on condition of the semiconductor device, and generating the first and the second control signals having substantially the same voltages as the power supply voltage and the third control signal of the high voltage, respectively, when the high voltage is applied to the pad of the semiconductor device under a power off condition of the semiconductor device;

an output buffer including first and second pull-up transistors connected in series between the power supply voltage and the pad, first and second pull-down transistors connected in series between the pad and the ground voltage, a pre-driver for pulling up or down a voltage of the pad in response to an input signal when an output enable signal is enabled and for switching off the first and second pull-up transistors and the first and second pull-down transistors when the output enable signal is disabled, and a first tolerance and current blocking means for adjusting voltage differences between respective gates and respective sources/drains of the first and second pull-up transistors and the first and second pull-down transistors to be below a predetermined voltage level in response to the first, second and third control signals, and preventing current flow from the pad to the power supply voltage if the high voltage is applied to the pad under power on or power off conditions; and

an input buffer including a transmission gate for transmitting an input signal applied to the pad to a first node in response to the first control signal, a third, a fourth and a fifth pull-up transistors connected in series between the power supply voltage and a second node and having corresponding gates connected to a third node, the pad and the first node, respectively, a third pull-down transistor connected between the second

node and the ground voltage and having a gate connected to the first node, a second tolerance and current blocking means for adjusting voltage differences between respective gates and respective sources/drains of the third, fourth and fifth pull-up transistors and the third pull-down transistor to be below a predetermined voltage in response to the first and third control signals, and preventing current flow from the pad to the power supply voltage if the high voltage is applied to the pad under either the power on or power off conditions.

2. The input and output circuit as set forth in claim 1, wherein the control signal generating means comprises:

a first circuit for generating the first control signal of the power supply voltage and the second control signal of the ground voltage if the high voltage is applied to the pad under a power on condition, and generating the first control signal and the second control signal which have substantially the same voltage as the power supply voltage if the high voltage is applied to the pad under a power off condition; and

a second circuit for generating the third control signal of the high voltage if the high voltage is applied to the pad under the power on or power off conditions.

3. The input and output circuit as set forth in claim 2, wherein the first circuit comprises:

first and second PMOS transistors connected in series between the power supply voltage and a fourth node, having corresponding gates connected to the second control signal and the power supply voltage, respectively, and substrates connected to the first control signal;

a first NMOS transistor connected between the second control signal and the ground voltage and having a gate connected to the power supply voltage;

a third PMOS transistor connected between the second control signal and the first control signal, having a gate connected to the power supply voltage, and substrate connected to the first control signal; and

a first voltage drop circuit for dropping the voltage of the pad down when the voltage of the pad is greater than a voltage of the fourth node.

4. The input and output circuit as set forth in claim 2, wherein the second circuit comprises:

a fourth, a fifth and a sixth PMOS transistors connected in series between the power supply voltage and the pad, having corresponding gates connected to a fifth node, the pad and the first control signal, respectively, and substrates connected to the third control signal;

a seventh PMOS transistor connected between the fifth node and the first control signal, having a gate connected to the power supply voltage and a substrate connected to a common node of the fourth and fifth PMOS transistors; and

a second NMOS transistor connected between the fifth node and the ground voltage and having a gate connected to the power supply voltage.

5. The input and output circuit as set forth in claim 1, wherein the pre-driver generates a first, a second and a third signals for controlling the first tolerance and current blocking means.

6. The input and output circuit as set forth in claim 5, wherein the first tolerance and current blocking means comprises:

a first driver including a switching transistor for transmitting the power supply voltage to a sixth node in response to the second control signal by being turned on under the power on condition, a sixth pull-up transistor connected between the sixth node and a seventh node, having a gate connected to the first control signal and a substrate connected to the third control signal, and a fourth pull-down transistor connected between the seventh node and the ground voltage and having a gate connected to the first signal;

a second driver including a seventh pull-up transistor and a fifth pull-down

transistor connected in series between the power supply voltage and the ground voltage and having corresponding gates connected to the third signal;

a third driver including a backward diode connected between the power supply voltage and an eighth node, an eighth pull-up transistor connected between the eighth node and a ninth node, having a gate connected to the second signal and a substrate connected to the third control signal, a sixth pull-down transistor connected between a tenth node and the ground voltage and having a gate connected to the second signal, and first and second transmission transistors connected in series between the ninth node and the tenth node and having corresponding gates connected to the first control signal for transmitting a signal to an eleventh node;

a first transistor connected between the seventh node and the first control signal, having a gate connected to the power supply voltage and a substrate connected to the third control signal, for making the seventh node have substantially the same voltage as the power supply voltage under the power off condition;

a second transistor connected between the eleventh node and the pad, having a gate connected to the first control signal and formed on a substrate connected to the third control signal, for transmitting the high voltage applied to the pad to the eleventh node under the power on or power off conditions;

a second voltage drop circuit for lowering the high voltage applied to the pad; and

a third transistor connected between the common node of the first and second pull-up transistors and the second voltage drop circuit, having a gate connected to the second signal and a substrate connected to the third control signal, for lowering a voltage of the common node of the first and second pull-up transistors if the high voltage is applied to the pad under the power on or power off conditions.

7. The input and output circuit as set forth in claim 6, wherein the switching transistor is a PMOS transistor.

8. The input and output circuit as set forth in claim 6, wherein the

backward diode is a PMOS transistor.

9. The input and output circuit as set forth in claim 6, wherein the first and second transmission transistors are NMOS transistors.

10. The input and output circuit as set forth in claim 6, wherein the first, second and third transistors are PMOS transistors.

11. The input and output circuit as set forth in claim 1, wherein the second tolerance and current blocking means comprises:

a fourth transistor connected between the third node and the ground voltage and having a gate connected to the power supply voltage, for making the third node have the ground voltage under the power on condition;

a fifth and sixth transistors connected in series between the third node and the first node, having corresponding gates connected to the power supply voltage, and substrates connected to the third control signal, wherein a common node thereof is connected to the common node of the third and fourth pull-up transistors, for transmitting a voltage of the first node to the third node and the common node of the third and fourth pull-up transistors under power on condition; and

a seventh transistor connected between the common node of the fourth and fifth pull-up transistors and the first node, having a gate connected to the power supply voltage and a substrate connected to the third control signal, for transmitting the voltage of the first node to the common node of the fourth and fifth pull-up transistors.

12. The input and output circuit as set forth in claim 11, wherein the fourth transistor is an NMOS transistor.

13. The input and output circuit as set forth in claim 11, wherein the fifth, sixth and seventh transistors are PMOS transistors.

14. An input and output circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a first control signal of a power supply voltage level, a second control signal of a ground voltage level and a third control signal of a high voltage level when the high voltage is applied to a pad of the semiconductor device under a power on condition and for generating the first and second control signals of a voltage level similar to the power supply voltage and the third control signal of the high voltage level when the high voltage is applied to the pad under a power off condition; and

an output buffer including first and second pull-up transistors connected in series between the power supply voltage and the pad, first and second pull-down transistors connected in series between the pad and the ground voltage, a pre-driver for pulling up or down a pad voltage of the pad in response to an input signal if an output enable signal is enabled and for switching off the first and second pull-up transistors and the first and second pull-down transistors if the output enable signal is disabled, and a tolerance and current blocking means for adjusting voltage differences between respective gates and respective sources/drains of the first and second pull-up transistors and the first and second pull-down transistors to be below a predetermined voltage in response to the first, second and third control signals, and preventing current flow from the pad to the power supply voltage if the high voltage is applied to the pad under either the power on or the power off conditions.

15. The input and output circuit as set forth in claim 14, wherein the pre-driver generates first, second and third signals for controlling the tolerance and current blocking means.

16. The input and output circuit as set forth in claim 15, wherein the tolerance and current blocking means comprises:

a first driver including a switching transistor for transmitting the power supply

voltage to a first node in response to the second control signal by being turned on under the power on condition, a third pull-up transistor connected between the first node and a second node, having a gate connected to the first signal and a substrate connected to the third control signal, and a third pull-down transistor connected between the second node and the ground voltage and having a gate connected to the first signal;

a second driver including a fourth pull-up transistor and a fourth pull-down transistor connected in series between the power supply voltage and the ground voltage and having corresponding gates connected to the third control signal;

a third driver including a backward diode connected between the power supply voltage and a third node, a fifth pull-up transistor connected between the third node and a fourth node, having a gate connected to the second signal and a substrate connected to the third control signal, a fifth pull-down transistor connected between a fifth node and the ground voltage and having a gate connected to the second signal, and first and second transmission transistors connected in series between the fourth node and the fifth node and having corresponding gates connected to the first control signal for transmitting a signal to a sixth node;

a first transistor connected between the second node and the first control signal, having a gate connected to the power supply voltage and a substrate connected to the third control signal, for making the second node have substantially the same voltage level as the power supply voltage under the power off condition;

a second transistor connected between the sixth node and the pad, having a gate connected to the first control signal and a substrate connected to the third control signal, for transmitting the high voltage applied to the pad to the sixth node;

a voltage drop circuit for lowering the high voltage applied through the pad; and

a third transistor connected between the common node of the first and second pull-up transistors and the voltage drop circuit, having a gate connected to the second signal and a substrate connected to the third control signal, for lowering a voltage of the common node of the first and second pull-up transistors if the high voltage is applied to the pad under the power on or power off conditions.

17. The input and output circuit as set forth in claim 16, wherein the switching transistor is a PMOS transistor.

18. The input and output circuit as set forth in claim 16, wherein the backward diode is a PMOS transistor.

19. The input and output circuit as set forth in claim 16, wherein the first and second transmission gates are NMOS transistors.

20. The input and output circuit as set forth in claim 16, wherein the first, the second and the third transistors are PMOS transistors.

21. An input and output circuit of a semiconductor device, comprising:

a control signal generating means for generating a first control signal of power supply voltage, a second control signal of ground voltage and a third control signal of a high voltage greater than the power supply voltage, respectively, if the high voltage is applied to a pad of the semiconductor device under a power on condition of the semiconductor device, and generating the first and the second control signals having substantially the same voltage as power supply voltage and the third control signal of the high voltage if the high voltage is applied to the pad of the semiconductor device under a power off condition of the semiconductor device; and

an input buffer including a transmission gate for transmitting an input signal applied to the pad to a first node in response to the first control signal, first, second and third pull-up transistors connected in series between the power supply voltage and a second node having corresponding gates connected to a third node, the pad and the first node, respectively, a first pull-down transistor connected between the second node and the ground voltage and having a gate connected to the first node, a tolerance and current blocking means for adjusting voltage differences between respective gates and

respective sources/drains of the first, second and third pull-up transistors and the first pull-down transistor to be below a predetermined voltage value in response to the first and second control signals, and preventing current flow from the pad to the power supply voltage if the high voltage is applied to the pad under either the power on or power off conditions.

22. The input and output circuit as set forth in claim 21, wherein the tolerance and current blocking means comprises:

a first transistor connected between the third node and the ground voltage and having a gate connected to the power supply voltage, for increasing a voltage level of the third node to the power supply voltage under the power on condition;

a second and third transistors connected in series between the third node and the first node, having corresponding gates connected to the power supply voltage and formed on a semiconductor substrate connected to the second control signal, wherein a common node thereof is connected to a common node of the first and second pull-up transistors, for transmitting the voltage of the first node to the common node of the first and second pull-up transistors under the power off condition; and

a fourth transistor connected between the common node of the second and third pull-up transistors and the first node, having a gate connected to the power supply voltage and a substrate connected to the second control signal, for transmitting the voltage of the first node to the common node of the second and third pull-up transistors under the power off condition.

23. The input and output circuit as set forth in claim 21, wherein the first circuit is an NMOS transistor.

24. The input and output circuit as set forth in claim 21, wherein the second, third and fourth transistors are PMOS transistors.

25. An input and output circuit of a semiconductor device, the circuit comprising:

a control signal generating portion for generating a first control signal of a power supply voltage level, a second control signal of a ground voltage level and a third control signal of a high voltage level when the high voltage is applied to a pad of the semiconductor device under a power on condition and for generating the first and second control signals of a voltage level similar to the power supply voltage and the third control signal of the high voltage level when the high voltage is applied to the pad under a power off condition; and

at least one output buffer comprising at least one pull-up transistor connected between the power supply voltage and the pad, at least one pull-down transistor connected between the pad and the ground voltage, and a tolerance and current blocking portion for adjusting voltage differences between respective gates and respective sources/drains of the at least one pull-up transistor and the at least one pull-down transistor to be below a predetermined voltage in response to the first, second and third control signals, and preventing current flow from the pad to the power supply voltage if the high voltage is applied to the pad under either the power on or the power off conditions.